A Review on Crosstalk in On-Chip High Speed VLSI Interconnects

Hitlendra Pratap Singh[1] , Dr. G.S. Virdi[2]
[1]Dept. of ECE, MIET, Meerut, India-250005
[2]GGSCMT Mohali, India-140301

Abstract- *As process technologies scale into deep submicrometer wiring in this environment introduces resistive, capacitive, and inductive parasitics. When the operating clock frequency is used beyond GHz in on-chip environment then Crosstalk, crosstalk delay, speed, energy consumption, signal integrity, and reliability affects due to these parasitics. On-chip signal crosstalk is a function of switching activity pattern, coupling parasitics, and signal timing.*

Indext Terms- *Wires Parasitic, Bus, Crosstalk, Crosstalk delay, CACs, Interconnect.*

1. Introduction

In DSM and UDSM technology environment due to scaling of devices and speed of circuit is increasing because of yearly change in technology, the parasitic effect introduces in On-chip interconnect wires which dominate relevant metrics of digital integrated circuits such as speed, energy consumption, delay , crosstalk , and signal integrity. The average length of interconnect wire is increasing yearly in comparison to device dimension. Therefore, careful investigation of crosstalk, dealy, and power consumption is required in On-Chip VLSI interconnect. To investigate these parameters interconnect can be modeled as capacitive, resistive, and inductive parasitic. Interconnect parasitics like capacitance, resistance, and inductance are not included in a single physical point but are distributed over the entire length of the wire. A fully fledged circuit model that illustrate all the parasitic capacitance, resistance, and inductance of the interconnections is shown in below figure (1) and a circuit model with capacitive only parasitic shown in figure (2).

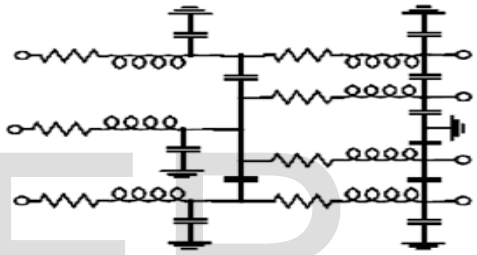

Figure (1) Wire model with full-fledged parasitic [25]

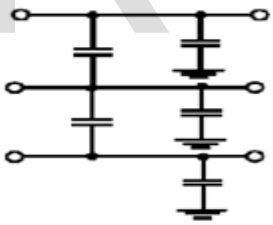

Figure (2) Wire model with capacitive parasitic [25]

consider first a simple rectangular wire placed above the semiconductor substrate, as shown in Figure (3). If the width of the wire is substantially larger than the thickness of the insulating material, it may be assumed that the electrical-field lines are orthogonal to the capacitor plates, and that the parallel-plate capacitor model can model its capacitance also called area capacitance.

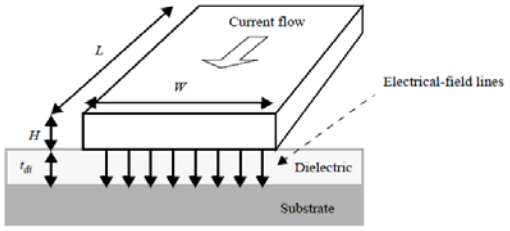

Figure (3) Parallel plate capacitance model of Interconnect wire [25]

The model shown in figure (4) decomposes the capacitance into two contributions: a parallel plate capacitance, and a fringing capacitance, modeled by a cylindrical wire with a diameter equal to the thickness of the wire

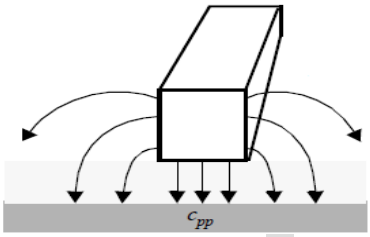

Figure (4) Fringing fields [25]

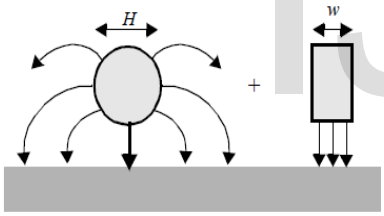

Figure (5) Model of fringing field capacitance [25]

As per the International technology roadmap for semiconductors (ITRS), the packing density is increasing year by year and technology scale down to beyond nanometer scale and will contain more than billion transistors and operate well beyond clock speed 10GHz. Therefore, transmition of power signal, ground signal, clock, data, address, and other control signals through interconnects in such a high speed , high complexity environment the signals from one lines to another lines affect each other because in this environment interconnect behaves as a transmission line and modeled as RLC or RC type circuit network. Due to crosstalk delay, signal integrity, and power consumption deficiencies will arise. The components, which affect the behavior of the on-chip bus these are mainly internal parasitic capacitances of the transistor, interconnect capacitances, and input capacitances of the fan out gates. To simplify the parasitic capacitance model of interconnect it contains mainly three capacitances C_a area capacitance to substrate , C_f fringe or side-wall capacitance to substrate , and C_c cross-coupling capacitance between two adjacent shapes which shown in figure (5).

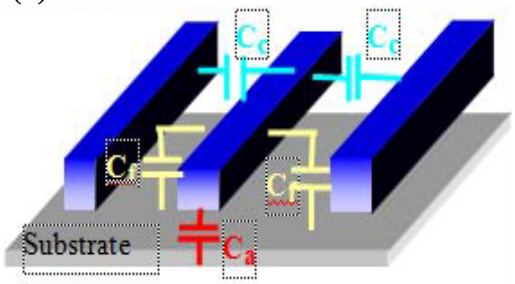

Figure (5) parasitic capacitance model

2. Crosstalk

Crosstalk is an unwanted coupling from a neighboring signal wire to a network node introduces an interference that is generally called crosstalk and the resulting disturbance acts as a noise. This can be of both inductive and capacitive type coupling. This is illustrated in figure (6). The coupling between the groups of the three wires is classified into five Types depending upon the nature of transitions of signals in the wire that are Type-0, Type-1, Type-2, Type-3 and Type-4. This is illustrated in Table (1). Where $\gamma = C_c/C_l$ (i.e. ratio of coupling capacitance to load capacitance).

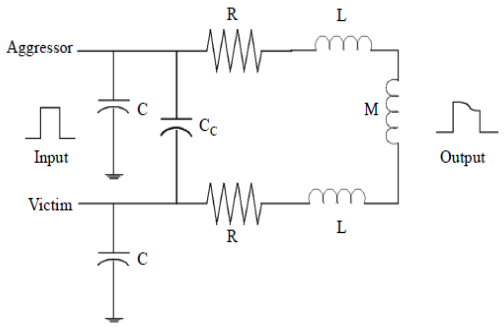

Figure (6) Effect of RLC interconnect model

Table (1) Crosstalk Classes and Corresponding Delays:

Crosstalk Class	**Transition Patterns (d_{k-1}, d_k, d_{k+1})**	**Crosstalk**
1	↑−↑, ↓−↓, ↑−↓, ↓−↑, ↑−−, −−↓, −−−, −−↑, ↓−−	**0**
2	**- - -,** ↑↑↑, ↓↓↓	**1**
3	- - ↑, ↑ - - , - - ↓, ↓ - - , ↑↑−, ↓↓−, −↑↑, −↓↓	1+γ
4	−↑−, ↑ - ↑, ↑ - ↓, −↓−, ↓ - ↓, ↓ -↑, ↓↓↑, ↑↑↓, ↓↑↑, ↑↓↓	1+2γ
5	−↓↑, −↑↓, ↑↓−, ↓↑−	1+3γ
6	↓↑↓, ↑↓↑	1+4γ

***The symbols ↑, ↓, − are used to indicate 0→1, 1→0 and 1→1 (or) 0→0 transitions**

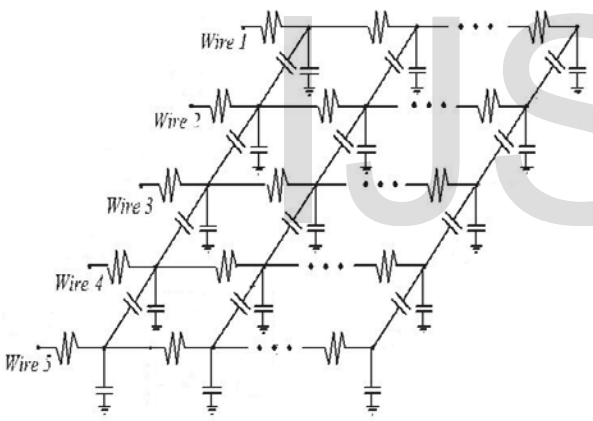

Figure (7) Distributed RC model for five wires [5]

Crosstalk problems arise due to on-chip crosstalk between neighboring wires, which becomes more pronounced at deep submicron regime. Crosstalk occurs when a signal on a wire (aggressor) affects the signal on a neighboring wire (victim) due to capacitive and inductive coupling between neighboring wires. Crosstalk may cause violation of timing constraints by hastening or delaying the signal transition or logic failure by inducing a glitch or spurious signal transition on the victim wire crosstalk is a function of coupling

TABLE (2) SUBCLASSIFICATION OF PATTERNS BY SIGNAL EXPRESSIONSON WIRE 3 IN A FIVE-WIRE BUS [5]

Subclass *k*	Patterns	Subclass *k*	Patterns
1	↑↑↑↑↑	13	- -↑- -, ↑-↑-↓, ↓-↑-↑
2	-↑↑↑↑, ↑↑↑↑-		-↑↑↓-, ↑↑↑↓↓, ↓↑↑↓↑
3	↑-↑↑↑, ↑↑↑-↑		-↓↑↑-, ↑↓↑↑↓, ↓↓↑↑↑
4	-↑↑↑-, ↓↑↑↑↑, ↑↑↑↑↓	14	- -↑-↓, ↓-↑- -, -↑↑↓↓, ↓↑↑↓-, -↓↑↑↓, ↓↓↑↑-
5	- -↑↑↑, ↑↑↑- -, -↑↑-↑, ↑-↑↑-	15	↓-↑-↓, ↓↑↑↓↓, ↓↓↑↑↓
		16	↓↓↑-↓, ↓-↑↓↓
6	↑-↑-↑, ↑↑↑↓↑, ↑↓↑↑↑	17	- -↑↓↓, ↓↓↑--, -↓↑-↓, ↓-↑↓-
7	-↑↑↑↓, ↓↑↑↑-	18	- -↑↓-, -↓↑- -, ↑-↑↓↓, ↑↓↑-↓, ↓-↑↓↑, ↓↓↑-↑
8	- -↑↑-, -↑↑--, ↓-↑↑↑, ↓↑↑-↑, ↑-↑↑↓, ↑↑↑-↓	19	- -↑↓↑, ↑↓↑--, -↓↑-↑, ↑-↑↓-
9	↓↑↑↑↓	20	↑-↑↓↑, ↑↓↑-↑
10	- -↑↑↓, ↓↑↑- -, -↑↑-↓, ↓-↑↑-	21	↓↓↑↓↓
		22	↓↓↑↓-, -↓↑↓↓
11	↓-↑↑↓, ↓↑↑-↓	23	-↓↑↓-, ↑↓↑↓↓, ↓↓↑↓↑
12	- -↑-↑, ↑-↑--, -↑↑↓↑, ↑↑↑↓-, -↓↑↑↑, ↑↓↑↑-	24	↑↓↑↓-, -↓↑↓↑
		25	↑↓↑↓↑

capacitances, driver strengths, and signal timing characteristics.
In figure (7), a new analytical five-wire delay model is proposed in which two extra neighboring wires are included in the RC interconnect model which gives better accuracy than the 3-wire RC interconnect model.

3. Literature Review

The performance of interconnect drivers degrade due to reliability mechanisms such as bias temperature instability
(BTI) and hot carrier injection (HCI) depends on the length and width of an interconnect wire. The dependence of bias temperature instability (BTI) and hot carrier injection (HCI)-induced frequency degradation on interconnect length has been examined for the first time [1]. To cope with crosstalk delay accurate delay models of coupled interconnects are needed. In particular, delay models based on analytical approaches are desirable, because they are not only largely transparent to technology, but also explicitly establish the connections between delays of coupled interconnects and transition patterns, thereby enabling crosstalk alleviating techniques such as crosstalk avoidance codes**.** An equalized on-chip global link structure was proposed employing a tapered CML driver, CTLE, and SA-based latch. Applying SQP nonlinear optimization methods for a driver–receiver cooptimization demonstrated the lowest energy/bit for the global link performance [2]. With Fourier series and Fourier integrals, a new and systematic approach, called the Amir and Nasser (AMN) method, is proposed to derive exact analytical expressions for step input response of distributed resistance capacitance (RC), inductance-capacitance (LC), and resistance-inductance capacitance (RLC) models of interconnects [3].

Crosstalk avoidance codes (CACs) used to alleviate the crosstalk delays by restricting the transition patterns on a bus. This paper proposed more number of crosstalk classes as compared to previous crosstalk classes as the delays of its classes do not overlap, both leading to more accurate control of delays and reduced delays and improved throughput. This crosstalk class has wider variety of tradeoff between bus delays and efficiency [4]. A realizable-II model for the driving-point impedance of an *RLC* current-mode transmission line is derived. The output current of an *RLC* current-mode transmission line is also derived. The model is extended to multiple parallel coupled interconnects with inductive and capacitive coupling between them In current-mode signaling the major difference over voltage-mode is the resistive termination at the receiver end. Accurate and efficient models are needed for current-mode signaling for issues such as energy dissipation and propagation delay. In voltage-mode signaling, the dynamic energy dissipation has traditionally been obtained from the well-known equation $E = CV^2_{dd}$, where C is the total capacitance [5].
3-D interconnect techniques in multilayer very large scale integration design, such as stacked layers and various chip stacking systems, have paved the way for the improvement of integrated circuit density and operation speed. However, these techniques often accompany with impedance discontinuities that induce signal integrity (SI)/power integrity and electromagnetic interference effects in this paper a no conformal domain decomposition method with second-order transmission condition for SI analysis of high-speed interconnects on a multi scale multilayer printed circuit board is proposed [6]. Over the past two decades, wire widths of interconnects have reduced by two orders of magnitude and at the same time the device density on the chips has increased by more than five orders of magnitude. Consequently, the current density in signal wires has increased, thereby making them extremely vulnerable to electro-migration (EM) failures. EM is a process in which mass transport takes place because of interaction between the moving electrons and the metal ions at high current densities. Migration of metal ions results in metal build-up or depletion resulting in catastrophic disconnections in the form of hillocks and voids. An improved and efficient method for static estimation of average and root-mean-squared currents used for electro migration (EM) reliability analysis is presented in this work. Significantly different from state-of-the-art, the

proposed method gives closed-form expressions for average and RMS currents in one complete cycle. The proposed method can be readily configured to work with different combinations of ramp and exponential waveforms [7].

To minimize worst-case crosstalk patterns in bus lines by using simulated annealing (SA)-based high-level synthesis solutions for a given data environment with correlations that do not result in such worst-case patterns. Besides synthesis moves, bus re-ordering and data transfer invert encoding is incorporated [8]. Fast waveform estimation (FWE) technique is used to estimate the output waveform for general RC interconnect networks in the presence coupling noise, while the static methods suffers from inaccuracy and instability to capture the non-monotonic nature of signal waveform in the presence of coupling noise. The accuracy of FWE is comparable to the general model order reduction based methods while maintaining an efficiency that is comparable to Elmore delay based analysis. FWE approach provides an efficiency that is comparable to like asymptotic waveform evaluation (AWE) [9].

To maximize quality while minimizing costs, the automotive engineer must uncover, understand, and eliminate crosstalk problems early in the design process, Closed-form estimates of worst or nearly worst case crosstalk can be useful in system analysis, since these estimates can quickly identify problem areas that require close inspection and they show a clear relationship between design parameters and crosstalk that allows intelligent modification of the system [10].

In DSM technology due to shrink in feature size of ICs CMOS gate driven interconnect become critical issues. Signal integrity (SI) is strongly affected by both the transmission line behavior of interconnects and the nonlinear behavior of CMOS drivers. Modeling of lossy interconnects with frequency-dependent line parameters has analyzed with FDTD and quite suitable for SI analysis in high-speed interconnect systems [11]. Crosstalk delay may be several times more than the delay of bus. The crosstalk delay has become a bottleneck in deep submicrometer system on chip designs. Crosstalk delay is reduced by skewing the timing signals on the bus, bus interleaving, precharging, or using repeaters. These solutions have varying degrees of success and are often technology dependent, power consuming or suitable to process variation. A technology independent solution to this problem is shielding which cuts the worst-case crosstalk delay by half, but it nearly doubles the wiring area [12]. Propagation delay across long on-chip buses is significant when adjacent wires are transitioning in opposite direction (i.e., crosstalk transitions) as compared to transitioning in the same direction. By employing Fibonacci, code it can be avoided [13]. A lie formula is used to convert the solution of the transmission line network into delay algebraic equations to obtain the time domain response. This algorithm can be used to model both identical and non-identical multiconductor lines and loads [14]. Crosstalk-induced latency is predicted by analyzing the possible crosstalk effects of adjacent patterns stored in an NOC router. Transition times of selected bits are then adjusted to relieve these predicted crosstalk-induced effects. It requires no extra wires comparison to shielding technique [15]. A utilitarian theory is proposed for multimetric optimization of delay, dynamic power, leakage power, and crosstalk noise, via gate sizing [16]. For fast and accurate modeling of the distributed *RLC* interconnect and transmission lines a closed forms of the state-space models and the recursive algorithms is used in this paper, which may be evenly or unevenly distributed. Considered models include the distributed *RLC* interconnect lines with or without external source and load connection. The importance is their modeling accuracy and very low computation complexity [17]. The crosstalk-induced delay, noise, and CMP-induced thickness-variation implications of dummy fill generated using rule-based wire track fill techniques and CMP-aware model-based methods for designs implemented in 65 nm process technology. The impact of fill metal is examined on several interconnect test structures, which provides important insights into the performance and reliability implications of both interlayer and interlayer capacitive coupling due to dummy fill and their effect on crosstalk-

induced delay and noise and then explore the crosstalk-induced timing, noise, capacitance, and CMP-induced thickness-variation implications of fill metal on several large-scale designs implemented in 65 nm process technology [18]. With depth analysis of signal slew and skew variation, the variations of rise/fall time and skew alter the behavior of coupled inductive lines under different switching patterns [19].A **2*π*** ***RLC*** interconnect model is used to investigate the effects of both coupling capacitance and mutual inductance on the crosstalk noise. Physical spacing and shield insertion are compared in terms of the coupling noise on the victim line for several technology nodes. a shield line can degrade rather than enhance signal integrity due to increased P/G noise coupling on the victim line [20]. Delay-noise strongly depends on the skew between the victim–aggressor driver input transitions, it is not possible a priori identify the victim-driver input transition that results in the worst-case delay-noise coupling capacitance accounts for more than 85% of the total interconnect capacitance [21]. Due to rapid scaling of process technologies has led to greatly improved performance at the cost of increased power consumption, most prominently leakage power. Dynamically pulsed MTCMOS with bus encoding for reduction of total power and crosstalk noise is proposed [22].

4. Conclusion

Crosstalk in on chip VLSI interconnects is a major issue when the operating clock frequency is beyond GHz range. Due to crosstalk delay, reliability, and power consumption affects.

5. Acknowledgment

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